REMARKS

Reconsideration and allowance of this application are respectfully requested in light of the above amendments and the following remarks.

Claims 5-12 are pending in this application. New claims 9-12 are previous claims 1-4 rewritten to more clearly define the invention. Claims 5-8 have been amended to accord proper dependency. Each of the claim amendments is for a reason unrelated to patentability, and no estoppel should be deemed to attach thereto.

Claims 1, 2, 5 and 6 were rejected under §102(b) as being anticipated by Ohsono (US Patent 5,831,310). Claims 3, 4, 7 and 8 were rejected under §103(a) as being obvious over Ohsono. Insofar as these rejections may be applied against new claims 9-12 and original claims 5-8, the Applicant respectfully traverses.

The inventions recited in claims 5-12 include structural features that achieve reduction of leakage current generation in a high voltage transistor. This is accomplished in a semiconductor transistor device wherein the diffusion layer of a second conductivity type has a two-layer structure comprising a source/drain diffusion layer and a source/drain side offset layer and the impurity concentrations between the source diffusion layer, the drain diffusion layer, the source side offset diffusion layer

and the drain side offset diffusion layer are defined with certain characteristics. Further, the positional relationship between the gate insulator film and the diffusion layer of the first conductivity type is formed such that the gate insulator film is not present below, but remains in contact with, the diffusion layer (claim 9) or the diffusion layer may be separated from the protruding regions of the gate insulator film (claim 10).

Ohsono discloses a semiconductor for checking the quality of a semiconductor region. The semiconductor comprises a plurality of ordinary low voltage transistors each having n-type source and drain regions, a gate oxide film and a gate electrode formed on the circuit element region. P-type channel stopper regions are formed on bottom portions of a field oxide film separated from the source and drain regions.

The Applicant traverses the rejection under §102(b) because Ohsono does not disclose, explicitly or inherently, each and every limitation of the Applicant's claimed invention. Claims 5-12 recite that "a source diffusion layer and a drain diffusion layer of a second conductivity type are formed on the region of the first conductivity type; a source side offset diffusion layer and a drain side offset diffusion layer of the second conductivity type are present around said source diffusion layer and said drain diffusion layer so as to be in contact therewith, respectively." The

structure contains a drain region having a two-layer structure. Ohsono does not disclose any offset diffusion layer. Thus, Ohsono does not anticipate the above-cited structural features relating to the offset diffusion layer.

Further, the claims recite that "regions at both ends, in a direction of a channel width, of said gate insulator film protrude from a boundary, in a lateral direction, between said source side offset diffusion layer and said drain side offset diffusion layer." Such structure is also not disclosed in Ohsono, which merely discloses the gate insulator film present only up to the boundary, between the source diffusion layer and the drain diffusion layer.

The claims also recite a "diffusion layer of the first conductivity type formed so as to surround said source side offset diffusion layer, said drain side offset layer and said gate insulator film so as to be in contact therewith." The Office Action proposes that the diffusion layer 82 in Ohsono (Figs. 2A and 2B) is in "contact with regions at both ends, in a direction of channel width, of a region where the gate insulator film is formed." However, the Applicant respectfully submits that Ohsono does not disclose such a structure. As is clearly shown in Ohsono (Figs. 2A and 2B), the diffusion layer 82 is separated from source and drain regions 83 and the gate insulator film 84. Further, this is explicitly stated in Ohsono col. 5 line 66 through col. 6 line

3, i.e., "channel stopper regions 82 are formed ... so as to be spaced apart from the n-type source and drain regions 83."

The Applicant also traverses the rejection under §103(a). It is well settled that a *prima facie* rejection of obviousness requires the prior art to disclose or suggest each and every feature of the claimed invention. Ohsono fails to disclose or even hint at the features of the Applicant's claimed invention as outlined above with respect to the rejection under §102.

Further, prior claims 3, 4, 7 and 8, now new and amended claims 11, 12, 7 and 8, respectively, are allowable based on their dependency from claims 1 and 2, which are allowable as discussed above.

For at least the above reasons, it is respectfully submitted that all grounds of rejection stated in the Office Action have been overcome. A Notice of Allowance is respectfully requested.

If any issues remain which may be best resolved through a telephone communication, the Examiner is requested to kindly telephone the undersigned at the local, Washington D.C. telephone number listed below.

Respectfully submitted,

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Exhibit I - Marked Up Claims

5. (Amended) A semiconductor device according to claim [1] 9 wherein said diffusion layer of the first conductivity type is a channel stopper region.

6. (Amended) A semiconductor device according to claim [2] 10 wherein said diffusion layer of the first conductivity type is a channel stopper region.

7. (Amended) A semiconductor device according to claim [3] 11 wherein said diffusion layer of the first conductivity type is a channel stopper region.

8. (Amended) A semiconductor device according to claim [4] 12 wherein said diffusion layer of the first conductivity type is a channel stopper region.